SGS-THOMSON MICROELECTRONICS

STV0196

QPSK/BPSK DEMODULATOR AND FEC IC

FRONT-END INTERFACE

- I AND Q 6 BITS DIGITAL INPUTS AT 2Fs
- QPSK DEMODULATION (Two Modes : A and B)
- INPUT SYMBOL FREQUENCY (Fs) UP TO 30MSYMBOLS/S
- DIGITAL NYQUIST ROOT FILTER : ROLL-OFF VALUE OF 0.35 IN MODE A
- DIGITAL CARRIER LOOP :
  - ON-CHIP DEROTATOR AND TRACKING LOOP
  - CARRIER OFFSET INDICATOR
  - LOCK DETECTOR
- DIGITAL TIMING RECOVERY :
  - INTERNAL TIMING ERROR EVALUATION AND FILTER
  - OUTPUT CONTROL SIGNAL FOR A 2Fs EXTERNAL VCO OR VCXO
- DIGITAL AGC :
  - INTERNAL SIGNAL POWER ESTIMATION AND FILTER
  - OUTPUT CONTROL SIGNAL FOR AGC (1 BIT PULSE DENSITY MODULATION)

FORWARD ERROR CORRECTION

- INNER DECODER :
  - VITERBI SOFT DECODER FOR CONVOLUTIONAL CODES, CONSTRAINT LENGTH M = 7, RATE 1/2
  - PUNCTURED CODES 1/2, 2/3, 3/4, 5/6 AND 7/8 IN MODE A
  - AUTOMATIC OR MANUAL RATE AND PHASE RECOGNITION
- DEINTERLEAVER :
  - WORD SYNCHRO EXTRACTION
  - CONVOLUTIVE DEINTERLEAVER
- OUTER DECODER :
  - IN MODE A : REED-SOLOMON DECODER FOR 16 PARITY BYTES ; CORRECTION OF UP TO 8 BYTE ERRORS
  - BLOCK LENGTHS : 204 IN MODE A
  - ENERGY DISPERSAL DESCRAMBLER

CONTROL

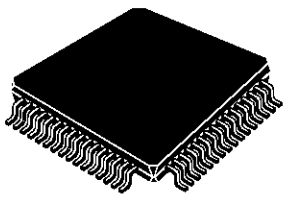
- I^2C SERIAL BUS

DESCRIPTION

Designed for the fast growing direct broadcast satellite (DBS) digital TV receiver market, the SGS-THOMSON STV0196 Digital Satellite Receiver Front-end integrates all the functions needed to demodulate incoming digital satellite TV signals from the tuner : Nyquist filters, QPSK/BPSK demodulator, signal power estimator, automatic gain control, Viterbi decoder, deinterleaver, Reed-Solomon decoder and energy dispersal descrambler. This high level of integration greatly reduces the package count and cost of a set top box. The demodulator blocks are suitable for a wide range of symbol rates while the advanced error correction functions guarantee a low error rate even with small receiver antennas or low power transmitters.

The STV0196 has multistandard capability.

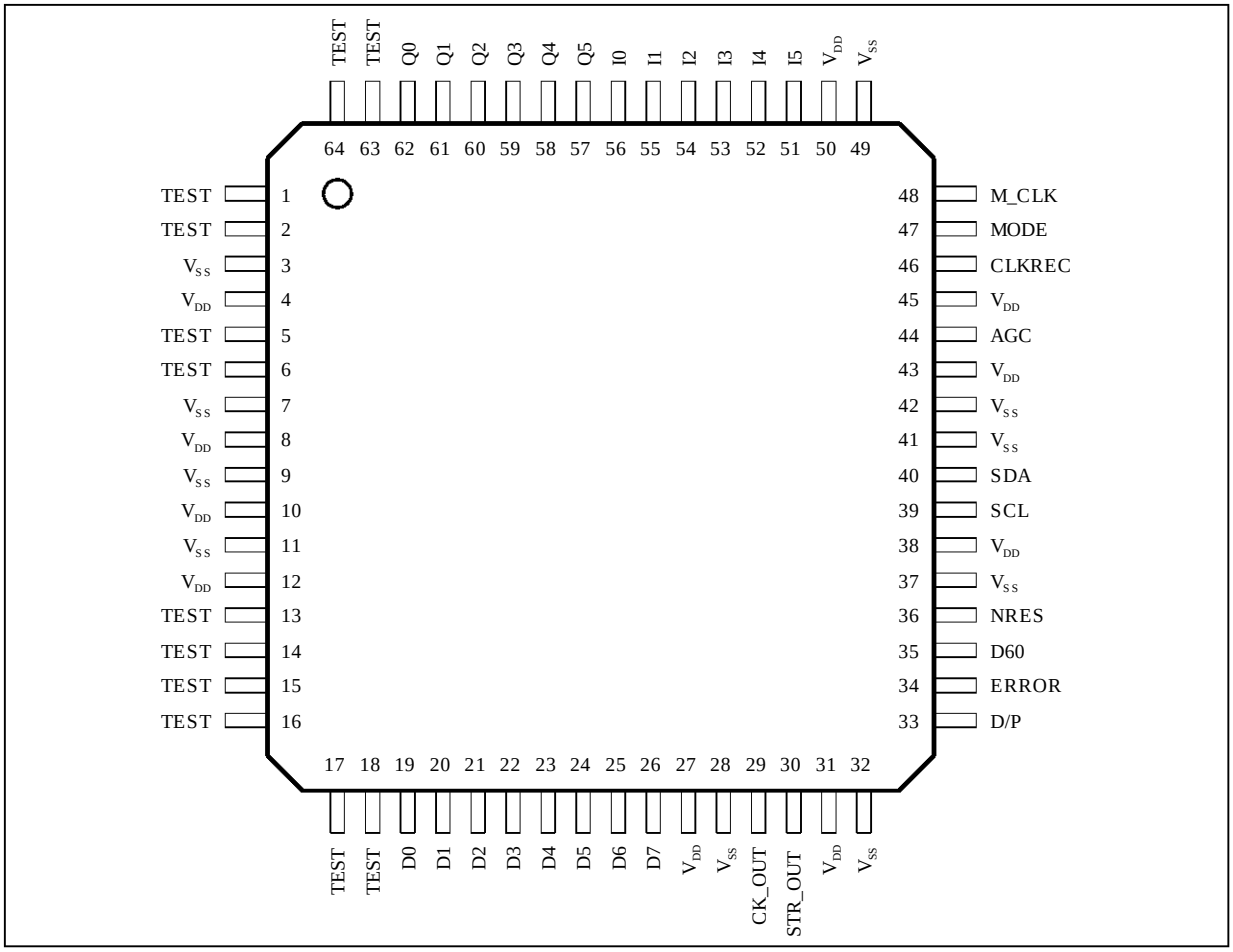
It is fully compliant with the recently defined Digital Video Broadcasting (DVB) standard (already adopted by satellite TV operators in the USA, Europe and Asia) and also compatible with the main consumer digital satellite TV standards in use.



PQFP64
(Plastic Package)

ORDER CODE : STV0196

PIN CONNECTIONS



PIN LIST

Pin Number	Pin Name	Type	Pin Description
SIGNAL INPUTS			
51, 52, 53, 54, 55, 56	I [5..0]	I	In Phase Component, at twice the symbol frequency (2Fs).
57, 58, 59, 60, 61, 62	Q [5..0]	I	In Quadrature Component, at twice the symbol frequency (2Fs).
48	M_CLK	I	Master Clock Input, 2Fs. Sampling Clock of the External A to D Converters.
FRONT END CONTROLS			
46	CLKREC	O	1 Bit Control Signal for the External CLK VCO. It must be Low-pass Filtered.
44	AGC	O	1 Bit Control Signal for the External AGC. It must be Low-pass Filtered.
35	D60	O	M_CLK Divided by 60
SIGNAL OUTPUTS			
26, 25, 24, 23, 22, 21, 20, 19	D [7..0]	O	Output Data
29	CK_OUT	O	Output Byte Clock
30	STR_OUT	O	Output Synchronization Byte Signal
33	D/P	O	Data/Parity Signal
34	ERROR	O	Output Error Signal. Set in Case of uncorrected Block.
I^2C MICRO INTERFACE			
39	SCL	I	Serial Clock
40	SDA	I/O	Serial Data Bus
OTHER			
47	MODE	I	0 = Mode A, 1 = Mode B
1, 2, 5, 6, 13, 14, 15, 16, 17, 18, 63, 64	TEST	O	Reserved for Manufacturing Test. It must remain unconnected
3, 7, 9, 11, 28, 32, 37, 41, 42, 49	V_{SS}	I	Ground References
4, 8, 10, 12, 27, 31, 38, 43, 45, 50	V_{DD}	I	3.3V Supply
36	NRES	I	Negative Reset

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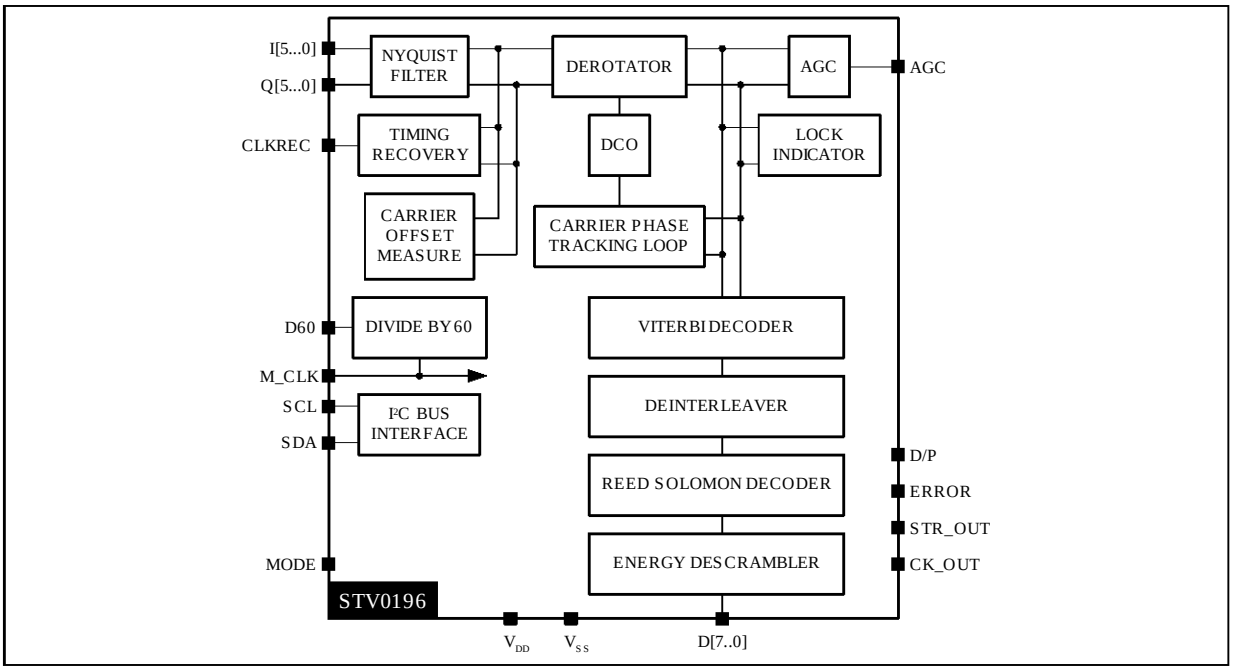
BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

I - I²C BUS SPECIFICATION

This is the standard I²C protocol.

The device address is "1101000" ; the first byte is therefore Hex D0 for a write operation and Hex D1 for a read operation.

I.1 - Write Operation

The first byte is the device address plus the direction bit (R/W = 0).
The second byte contains the internal address of the first register to be accessed.
The next byte is written in the internal register.
The following (if any) bytes are written in successive internal registers.

The transfer lasts until stop conditions are encountered.

The STV0196 acknowledges every byte transfer.

I.2 - Read Operation

The address of the first register to read is programmed in a write operation without data, and terminated by stop condition.

Then another start is followed by the device address and R/W = 1 ; all successive bytes are now data read at successive positions starting from the initial address.

The STV0196 acknowledges every byte transfer.

Example :

Write registers 0 to 3 with AA,BB,CC,DD

Start	Device Address, Write D0	ACK	Internal Address	ACK	Data AA	ACK	Data BB	ACK	Data CC	ACK	Stop

Read registers 2 and 3

Start	Device Address, Write D0	ACK	Register Address 01	ACK	Stop

Start	Device Address, Read D1	ACK	Data Read BB	ACK	Data Read CC	ACK	Stop

I.3 - Identification Register

This read only register gives the release number of the circuit in order to ensure software compatibility.

Internal Address : Hex 0B

1	0	0	0	0	0	0	1

Notes : - Unspecified register addresses must not be used.
- All the unused bits in the registers must be programmed to 0.

FUNCTIONAL DESCRIPTION (continued)

II - ADC INTERFACE

II.1 - M_CLK Master Clock Input

This is the highest frequency clock of the chip, at twice the symbol frequency; all other clocks are derived from it.
This clock should be output from an external VCO or VCXO, controlled by CLKREC output.
M_CLK divided by 60 is available to the system (output D60).

II.2 - I and Q Signal Inputs

Those signals are coded on 6 bits, either in 2's complement or as positive values : the choice is programmable via the Input Configuration register.
The $\pi/2$ ambiguity inherent in QPSK is solved in the Error Correction part.
A programmable bit in a mode register allows to multiply by -1 the data on Q input, in order to accommodate QPSK modulation with another convention of rotation sense ; (this is equivalent to a permutation of I and Q inputs, or a spectral symmetry).

III - NYQUIST ROOT FILTER

The I and Q components are filtered by a digital Nyquist root filter with the following features :
- Input : separate I and Q streams, two samples per symbol.
- Excess bandwidth : 0.35 in Mode A.
- The filters may be bypassed ; in this case, the input flow is connected to the carrier and clock recovery section.

Input Configuration Register

(the written value of each bit is the reset value)
Internal Address : Hex00

0	0	0	0	0	1	0	0
				BPSK(1), QPSK(0)	Nyquist filtering on (1)/off (0)	Signed (1) or positive (0) I&Q Inputs	-Q(1) or Q(0) input

IV - TIMING RECOVERY

The timing loop comprises an external VCO or VCXO, running at twice the symbol frequency, controlled by the output CLKREC ; this signal is a pulse density modulated output, at the symbol frequency, and represents the filtered timing error.

The loop is parametrised by two coefficients : alpha_tmg and beta_tmg ; the 12 bit filter output is converted into a pulse density modulation signal which should be filtered by an analog low pass filter before commanding the VCO.

IV.1 - Timing Loop Registers

Time Constant Register

Internal Address : Hex0C
Reset Value : Hex45

Istr	1	0	0	0	1	0	1
Invert bit	alpha_tmg (1 to 6)			beta_tmg (0 to 9)			

The bit "Istr" allows to change the polarity of the output signal, in order to accommodate both possibilities of external VCO :

Istr	Loop Control
0	VCO frequency raises when output average voltage raises
1	VCO frequency decreases when output average voltage raises

Timing Frequency Register

Internal Address : Hex0D

Signed number

The value of this register, when the system is locked, is an image of the frequency offset; it should be as close as possible to 0 in order to have a symmetric capture range ; reading it allows optimal trimming of the timing VCO range.

IV.2 - Loop Equations

The external VCO is controlled by the output CLKREC followed by a low pass filter.

The full analog swing of the output originates a relative frequency shift of $2\Delta f$, depending on the characteristics of the external VCO (typically a fraction of percent).

The frequency range is therefore $f = f_0 (1 \pm \Delta f)$.

Neglecting the analog low pass filter on the pulse modulated output, this loop may be considered as a second order loop.

FUNCTIONAL DESCRIPTION (continued)

The natural frequency and the damping factor may be calculated by the following formulas :

$$f_n = \frac{\omega_n}{2\pi} = \frac{F_s}{2\pi}\sqrt{\beta\, K_0\, K_d}$$

where β is programmed by the timing register : $\beta = 2^{beta\_tmg}$.

K_0 is the constant of the VCO : $K_0 = \frac{\Delta f}{2^{26}}$.

K_d is the phase detector ; its value depends on the roll-off value and on the power of the signal. : $K_d = 0.977m^2$ (in Mode A), or $K_d = 0.564m^2$ (in Mode B). where m is the programmed reference level (see AGC part), reset value : m = 24

F_s is the symbol frequency

Δf is the half range of the VCO

Therefore $f_n = 19.2\,10^{-6} \cdot m \cdot F_s \cdot \sqrt{\Delta f\, 2^{beta\_tmg}}$ (Mode A)

or $f_n = 14.6\,10^{-6} \cdot m \cdot F_s \cdot \sqrt{\Delta f\, 2^{beta\_tmg}}$ (Mode B)

The damping factor is : $\xi = \frac{\alpha}{2}\sqrt{\frac{K_0 K_d}{\beta}}$ with $\alpha = 2^{\,alpha\_tmg + 12}$

or $\xi = \frac{0.247 \cdot m \cdot \sqrt{\Delta f} \cdot 2^{alpha\_tmg}}{\sqrt{2^{\,beta\_tmg}}}$ (Mode A) or $\xi = \frac{0.188 \cdot m \cdot \sqrt{\Delta f} \cdot 2^{alpha\_tmg}}{\sqrt{2^{beta\_tmg}}}$ (Mode B).

beta_tmg can only take value from 0 to 9 ; if beta_tmg = 0, the loop becomes a first order one.

alpha_tmg can take any value from 1 to 6 ; if both alpha_tmg and beta_tmg are null, the loop is open ; the duty cycle of the CLKREC output is controlled by writting the timing frequency register.

The next curve shows the natural frequency for a symbol frequency of 20Mbd, in Mode A, with nominal reference level m = 24 as a function of the VCO relative frequency half range Δf, for different values of the register value beta_tmg.

The following chart gives the value of the damping factor as a function of the VCO relative range, for different combinations of alpha_tmg and beta_tmg, noticing that the damping factor only depends on the value of $\frac{\alpha}{\sqrt{\beta}}$ or (2 . alpha_tmg - beta_tmg).

FUNCTIONAL DESCRIPTION (continued)

Figure 1 : Natural Frequency for Fs = 20MBauds

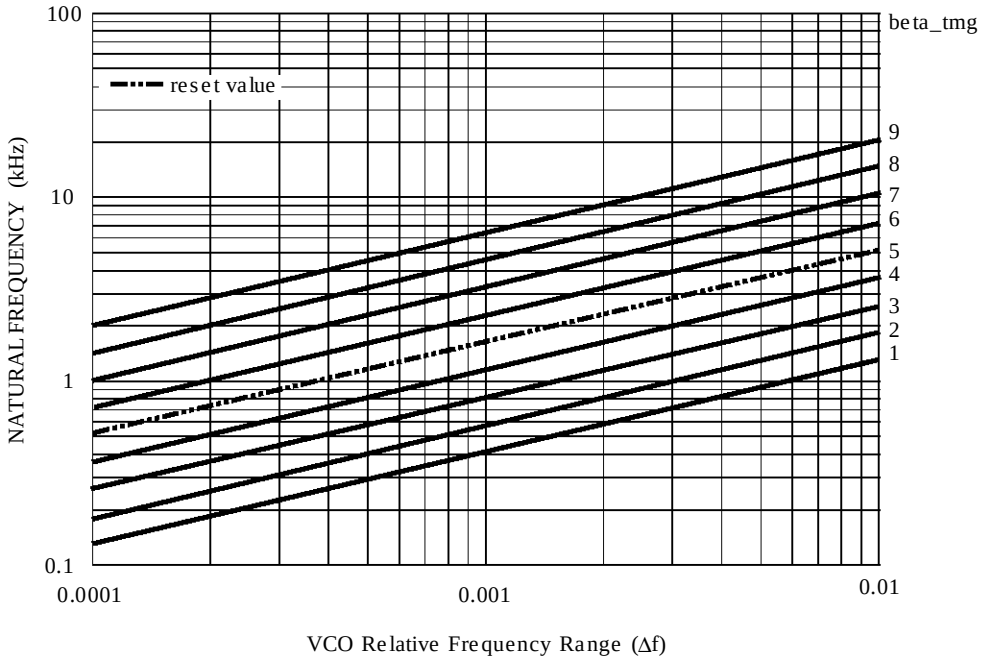

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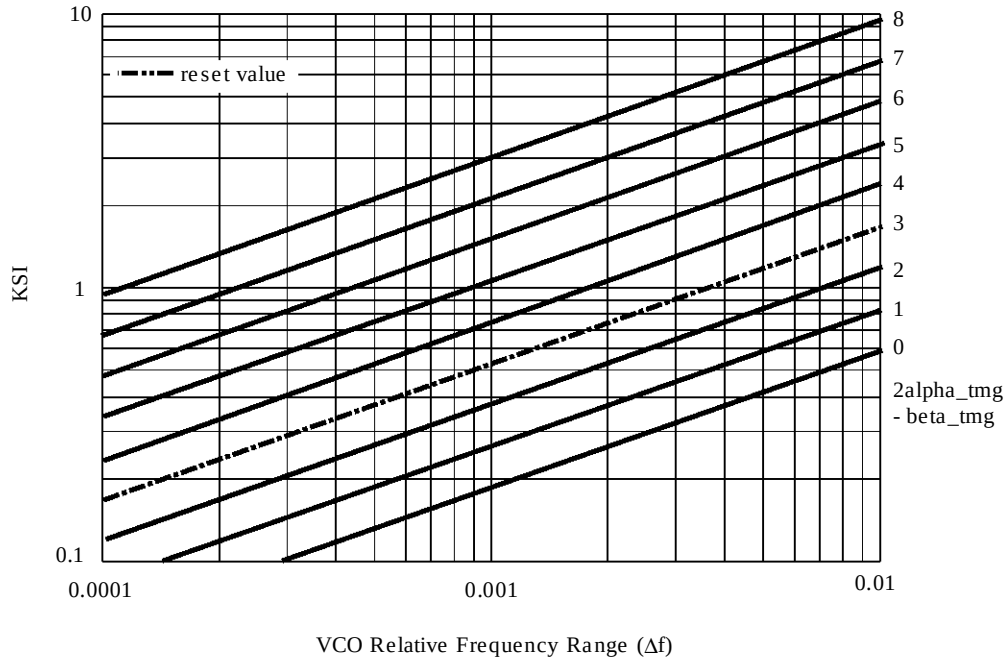
Figure 2 : Damping Factor



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Example :

the VCO is trimmed from 39.9MHz to 40.1MHz when the VCO control output CLKREC goes from duty cycle 0 to 100%. The peak-to-peak relative range is therefore 0.5% and $\Delta f = 0.0025$; the reset values of the parameters (alpha_tmg = 4, beta_tmg = 5) leads to a natural frequency of 2.6kHz, with a damping factor of 0.84.

FUNCTIONAL DESCRIPTION (continued)

V - CARRIER RECOVERY ; DEROTATOR

The input of the circuit is a pair of demodulated signals ; however, there may subsist some phase error not corrected by the front end loop.

Furthermore, the demodulation may be done at constant frequency; the tuner is trimmed in order to make the useful signal bandwidth centered on this demodulation frequency ; in that case, a carrier offset frequency may subsist; it is fixed by the mean of the on-chip derotator which acts as a fine tuning carrier loop.

The derotator frequency range is limited to an interval corresponding to $\pm F_S/16$.

V.1 - Loop Parameters

Like the timing loop, the carrier loop is a second order system where two parameters α and β may be programmed respectively with alpha_car and beta_car.

Carrier Loop Parameter Registers

Internal Address : Hex0E

1	0	1	0	0	0	1	1

Derotator ON/OFF — alpha_carrier — beta_carrier

Derotator Frequency Register

Internal Address : Hex0F

Signed number

This 8 bit R/W register may be written at any time to force the central frequency of the derotator to start the carrier research, or read, when the loop is locked,in order to know the current carrier offset (one LSB correspond to $F_S/2048$).

V.2 - Loop Equations

The natural pulsation is :

$$\omega_n = 10^{-3} \cdot f_s \cdot \sqrt{m \cdot 2^{beta\_car}}$$

and the damping factor is :

$$\xi = 0.128 \cdot 2^{alpha\_car} \cdot \sqrt{\frac{m}{2^{beta\_car}}}.$$

where m is the reference value (see AGC registers).

The next table gives for the nominal amplitude m = 24 the natural period (in symbols), and the damping factor for the possible values of alpha_car.

As an example, the corresponding natural frequency is given assuming a symbol frequency of 20MBauds.

The shaded area correspond to the reset values

beta_car (reg. value)	0	1	2	3	4	5	6	7
$T_n = 2\pi/\omega_n$ (symb per)	NA	907	642	454	321	227	160	113
f_n (kHz) for F = 20Mbd		22	31	44	62	88	125	177
alpha_car (reg. value)	Damping Factor							
0	NA	NA	NA	NA	NA	NA	NA	NA
1	NA	0.89	0.63	0.44	0.31	0.22	0.16	0.11
2	NA	1.77	1.25	0.89	0.63	0.44	0.31	0.22
3	NA	3.54	2.51	1.77	1.25	0.89	0.63	0.44
4	NA	7.09	5.01	3.54	2.51	1.77	1.25	0.89
5	NA	14.18	10.03	7.09	5.01	3.54	2.51	1.77

VI - CARRIER OFFSET EVALUATOR

An 8 bit register may be read at any time; it gives a signed value proportionnal to the carrier frequency offset according to the expression :

$$\Delta f = 1.8 \cdot 10^{-6} \cdot m^2 \cdot N \cdot F_S \text{ (in mode A)}$$

where F_S is the symbol frequency, m the symbol module (AGC reference), N the read value.

The maximum value for N is reached in nominal conditions for a carrier offset of 16% of F_S ; if greater, N remains saturated, giving a reliable sign indication over more than $\pm 50\%$ F_S range.

Carrier Offset Register

Internal Address : Hex10

Signed number

VI.1 - Lock Indicator

This 1 bit Carrier Found flag may be read (see Viterbi Status register) at any time ; it indicates that a QPSK signal is found, and that the carrier loop is closed ; This flag allows to detect false lock that can happen if the loop bandwidth is small regarding the frequency offset.

FUNCTIONAL DESCRIPTION (continued)

VII - AGC CONTROL

The modulus of the input is compared to a programmable threshold; the difference is scaled by the AGC coefficient, then integrated; the result is converted into a pulse density modulation signal to drive the AGC output ; it may be filtered by a simple analogue filter to control the gain command of any amplifier before the A to D converter.

The 8 integrator MSB's may be read or written at any time by the micro; when written, the LSB's are reset.

The integrator value is the level of the AGC output, after low pass filtering ; it gives an image of the input signal power, whatever this signal is, and can be used to point the antenna.

The coefficient may be reset by programmation; in that case, the AGC reduces to a programmable voltage synthesiser.

Control Registers

Internal Addresses : Hex11

Iagc	0	0	1	1	0	0	0
Invert signal	Reserved	AGC reference level ("m")					

Internal Addresses : Hex12

AGC integrator value (signed)

(Read/write register)

Internal Addresses : Hex13

0	0	0	0	0	0	1	0
Reserved					G[2..0] : AGC coefficient		

The 8 bit signed value in the integrator is the image of the AGC output; reading this value gives an image of the RF signal power.

A constant error on the modulus leads to a ramp at the output of the integrator with value :

$$AGC\_Int = 2^{AGC\_Coeff-16} \cdot error$$

As a consequence, for the reset conditions, a constant signal of null value (error = 24) should cause the output AGC duty cycle to go from 100% to 0% in 2^{22} symbol periods, or 8.7ms at 20MBauds.

If Iagc is set, the sign of the integrator is inverted.

VIII - VITERBI DECODER AND SYNCHRONIZATION

The convolutives codes are generated by the polynoms $Gx = 171_{oct}$ and $Gy = 133_{oct}$.

The Viterbi decoder computes for each symbol the metrics of the four possible paths, proportional to the square of the Euclidian distance between the received I and Q and the theoretical symbol value.

The puncture rate and phase are estimated on the error rate basis.

Five rates are allowed and may be enabled/disabled through register programming :
1/2, 2/3, 3/4,5/6, 7/8.

In Mode B, 7/8 is replaced by 6/7.

For each enabled rate, the current error rate is compared to a programmable threshold; if it is greater, another phase (or another rate) is tried until the good rate is obtained.

A programmable hysteresis is added to avoid to loose the phase during short term perturbation.

The rate may also be imposed by the external software, and the phase is incremented only on micro request ; the error rate may be read at any time in order to use other algorithm than implemented.

The decoder is accessed via a set of 9 registers :

Threshold Registers (VTH0 to VTH4)

Internal Address : Hex1 (VTH0) to 5 (VTH4)
Reset Value : Hex20

									Threshold Value
VTH0	0	Th6	Th5	Th4	Th3	Th2	Th1	Th0	rate 1/2
VTH1	0	Th6	Th5	Th4	Th3	Th2	Th1	Th0	rate 2/3
VTH2	0	Th6	Th5	Th4	Th3	Th2	Th1	Th0	rate 3/4
VTH3	0	Th6	Th5	Th4	Th3	Th2	Th1	Th0	rate 5/6
VTH4	0	Th6	Th5	Th4	Th3	Th2	Th1	Th0	rate 7/8 or 6/7

For each register, bits 6 to 0 represent an error rate threshold : the average number of errors happening during 256 bit periods; the maximum programmable value is 127/256 (higher error rates are of no practical use).

Puncture Rate Enable register

Internal Address : Hex09
Reset Value : Hex10 (Mode A)

0	0	0	E4	E3	E2	E1	E0

E4 : enable Punctured Rate 7/8 (Mode A) or 6/7 (Mode B)
E3 : enable Punctured Rate 5/6
E2 : enable Punctured Rate 3/4
E1 : enable Punctured Rate 2/3
E0 : enable Basic Rate 1/2

FUNCTIONAL DESCRIPTION (continued)

VIII - VITERBI DECODER AND SYNCHRONIZATION (continued)

Other Registers

VSEARCH

Internal Address : Hex06

A/M	F	SN [1..0]	TO [1..0]	H [1..0]

A/M : Automatic/manual

F : Freeze

SN [1..0] : Averaging period. It gives the number of bits required to calculate the rate error :

SN [1..0]	Number of bits
00	1.024
01	4.096
10	16.384
11	65.536

Reset Value : SN=01 (4096 bits)

TO [1..0] : Time out value. It programs the maximum duration of the synchro word research in automatic mode; if no sync is found within this duration, the phase is incremented.

TO [1..0]	Time out (in 1024 bit periods)
00	16
01	32
10	64
11	128

Reset Value : TO=10 (64K bit periods).

H [1..0] : Hysteresis value. It programs the maximum value of the Sync counter. The unit is the block duration (204 bytes in Mode A).

H [1..0]	Sync Counter max value (in blocks periods)
00	16
01	32
10	64
11	128

Reset Value : H=01 (32 blocks).

In Mode A, the sync word is 47hex and it is complemented to B8hex for every 8th block.

An Up/Down Sync counter counts whenever a sync word is recognized with the good timing, and counts down for each missing sync word ; this counter is bounded by a programmable maximum value; when this value is reached, the LK bit ("locked") is set in VSTATUS register; when the event counter counts down until 0, this flag is reset.

VSEARCH bit 7 (A/M) and bit 6 (F) programs the automatic/manual (or computer aided) search mode :

- if A/M =0 and F=0 : automatic mode; successive enabled punctured rates are tried with all possible phases, until the system is locked and the block synchro found ; this is the default (reset) mode.
- if A/M=0 and F=1, the current puncture rate is frozen, if no sync is found, the phase is incremented, but not the rate number; this mode allows to shorten the recovery time in case of noisy conditions: the puncture rate is not supposed to change in a given channel.
  In a typical computer aided implementation, the research begins in automatic mode; the micro reads the error rate or the PRF flag in order to detect the capture of a signal; then it switches F to 1, until a new channel is requested by the remote control.
- if AM=1 : manual mode; in this case, only one puncture rate should be validated, the system is forced to this rate, on the current phase, ignoring the time-out register and the error rate; in this mode, each 0 to 1 transition of the bit F leads to a phase incrementation, allowing full control of the operation by an external micro by choosing the lowest error rate :
  Reset Value : A/M=0, and F=0; automatic search mode

VERROR *(Read only register)*

Internal Address : Hex07

ERROR RATE

At any time, the last value of the error rate may be read in this register (unlike VTH, the possible range is 0 to 255/256).

VSTATUS *(Read only register)*

Internal Address : Hex08

CF	0	0	PRF	LK	PR [2..0]

CF : Carrier Found flag (see carrier recovery) CF when set, indicates that a QPSK signal is present at the input of the Viterbi decoder.

PRF : Puncture Rate Found
PRF indicates the state of the puncture rate research : 0 for searching, 1 when found ; this bit is irrelevant in manual mode.

LK : Locked/searching the sync word
LK indicates the state of the sync word research : 0 for searching, 1 when found.

PR [2..0] : Current Puncture Rate
It hold the current puncture rate indice with the correspondance :

Punctured Rate	Regiter Value PR[2..0]
Basic 1/2	100
Punctured 2/3	000
Punctured 3/4	001
Punctured 5/6	010
Punctured 7/8 (Mode A) or 6/7 (Mode B)	011

FUNCTIONAL DESCRIPTION (continued)

IX - CONVOLUTIONAL DE-INTERLEAVER

This is a 204 x 12 convolutional interleaver in Mode A ; the periodicity of 204 bytes for sync byte is preserved.
The de-interleaver may be skipped (see RS register).

X - REED-SOLOMON DECODER AND DESCRAMBLER

The input blocks are 204 byte long with 16 parity bytes in Mode A; the synchro byte is the first byte of the block.
Up to 8 byte errors may be fixed.

Code Generator polynom:

$$g(x) = (x - \omega^0)(x - \omega^1)(...)(x - \omega^{15})$$

over the Galois Field generated by :

$$X^8 + X^4 + X^3 + X^2 + 1 = 0$$

Energy dispersal descrambler :
Output energy dispersal descrambler generator :

$$X^{15} + X^{14} + 1$$

The polynom is initialised every eight blocks with the sequence 100101010000000. The synchro words are unscrambled.

Control register : RS register

Internal Address : Hex0A
The reset value is written in each register cell

7	6	5	4	3	2	1	0
1	0	1	1	1	0	0	0

RS7 : De-interleaver Enable
If 1, the input flow is deinterleaved.
If 0, the flow is not affected.

RS6 : If 0, Output data are corrected bytes (normal operating mode)
If 1, Output data are Reed-Solomon correction bytes (error count mode) (see Note 1)

RS5 : Reed-Solomon Enable
If 1, the input code is corrected.
If 0, no correction happens; all the data are fed to the descrambler.
The error signal remains inactive.

RS4 : Descrambler Enable
If 1, the output flow from Reed-Solomon decoder is descrambled.
If 0, the descrambler is desactived.

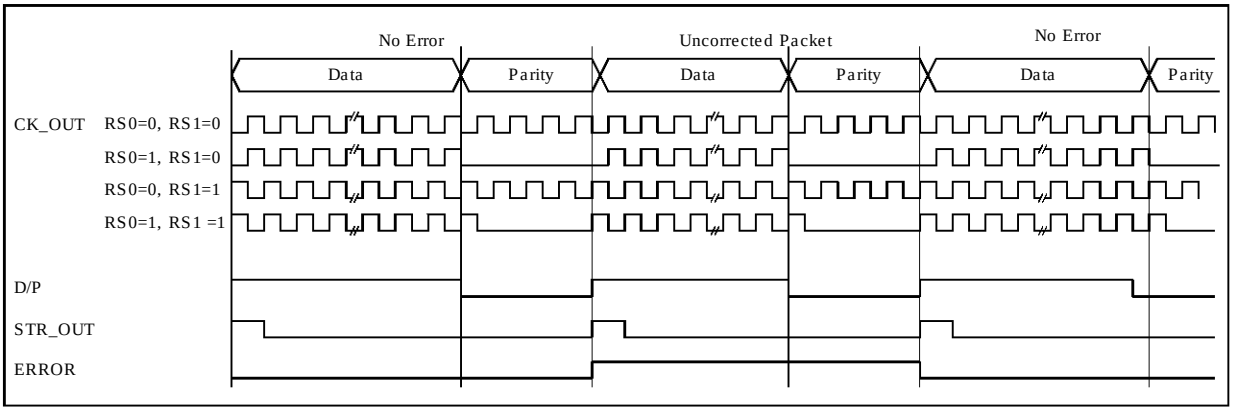
RS3 : Write Error Bit
If RS3=1, and uncorrectible error happens, the MSB of the first byte following the sync byte is forced to 1after descrambling.

RS1 : Output Clock Polarity
If RS1=0, data and control signals change during high to low transition of CK_OUT.
If RS1=1, they change during the low to high transition.

RS0 : Output Clock Configuration
If RS0=0, CK_OUT is continuous.
If RS0=1, CK_OUT remains low during the parity bits.

Note 1 : When RS6 = 1, the output data are the correction bytes applied to data incoming the Reed-Solomon block.
The number of bits at 1 in these output data represent therefore the number of errors remaining at the output of VITERBI decoder.
All null output data mean no error left after VITERBI decoding.

Figure 3



Note : In mode A, the synchro word at the output is hex47 on seven sucessive packets and hexB8 on the eighth packet.

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damages occur, continuous operation at these limits is not intended and should be limited to those conditions specified in section "DC Electrical Specifications".

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply (1)	-0.3 to 4	V
V_I	Voltage on Input pins (2)	-0.3 to V_{DD} + 0.3	V
V_o	Voltage on Output pins	-0.3 to V_{DD} +0.3	V
T_{stg}	Storage Temperature	-40 to +150	^oC
T_{oper}	Operating Temperature	0 to +85	^oC
P_D	Power Dissipation	1.5	W

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Notes : 1. All V_{DD} to be tied together
2. SCL, SDA, NRES Pins can be tied to 5V ± 10% with an impedance ≥ 2kΩ (remark in these conditions the input leakage current becomes higher than 10µA).

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V, T_{amb} = 25^{o}C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	$0^oC \le T_{oper} \le 70^oC$ $0^oC < T_{oper} < 85^oC$, M_CLK ≤ 55MHz	3.0 3.15	3.3 3.3	3.6 3.45	V V
I_{DD}	Average Power Supply Current	C_{LOAD} = 20pF on all outputs, M_CLK = 60MHz		300	480	mA
V_{IL} V_{IH}	Input Logic Low Voltage except M_CLK Input Logic High Voltage except M_CLK	M_CLK = 60MHz	-0.3 2.0		0.8 3.6	V V
V_{IL} V_{IH}	Input Logic Low Voltage for M_CLK Input Logic High Voltage for M_CLK	M_CLK = 60MHz	-0.3 2.2		0.8 3.6	V V
I_{LK}	Input Leakage Current	V_{IN} = 0V and V_{DD}			10	µA
C_{IN}	Input Capacitance			3.5		pF
V_{OL} V_{OH}	Output Logic Low Voltage Output Logic High Voltage	C_{LOAD} = 20pF, I_{LOAD} = 2mA, M_CLK = 60MHz	 2.4		0.5	V V

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Note : This product doesn't withstand the MIL 883C Norm at 2kV, but only at 1.5kV (all V_{DD} tied together).

TIMING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
PRIMARY CLOCK (see Figure 4)					
t_{M_CLK}	Master Clock Period $0^oC \le T_{oper} \le 70^oC$ Master Clock Period $0^oC < T_{oper} < 85^oC$	16.6 18.2			ns ns
t_{HIGH}	Clock High Time	6			ns
t_{LOW}	Clock Low Time	6			ns
t_R	Clock Rising Edge			4	ns
t_F	Clock Falling Edge			4	ns
I[5:0],Q[5:0] INPUT SPECIFICATIONS (see Figure 5)					
t_{SU}	I,Q stable before M_CLK	4			ns
t_H	I,Q stable after M_CLK	4			ns
D60 OUTPUT CHARACTERISTICS (see Figure 6)					
t_{60}	D60 period	(Tm_clk * 60) - 10		(Tm_clk*60) +10	ns
D[7:0],D/P,CK_OUT,STR_OUT,ERROR OUTPUT CHARACTERISTICS					
Bit RS1 = 1 in register RS (adr = 0x0A) (see Figure 7)					
t_{CKSU}	D[7:0],D/P,STR_OUT,ERROR stable before CK_OUT Falling Edge	32			ns
t_{CKH}	D[7:0],D/P,STR_OUT,ERROR stable after CK_OUT Falling Edge	32			ns
Bit RS1 = 0 in register RS (adr = 0x0A) (see Figure 8)					
t_{CKSU}	D[7:0],D/P,STR_OUT,ERROR stable before CK_OUT Rising Edge	32			ns
t_{CKH}	D[7:0],D/P,STR_OUT,ERROR stable after CK_OUT Rising Edge	32			ns

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I^2C BUS CHARACTERISTICS (see Figure 9)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL} V_{IH}	Input Logic Low Voltage Input Logic High Voltage	 See Note 1	-0.3 2.0		0.8 5.5	V V
V_{OL} V_{OH}	Output Logic Low Voltage Output Logic High Voltage	C_{LOAD} = 20pF, I_{LOAD} = 2mA, M_CLK = 60MHz, see Note 1	 2.4		0.5 5.5	V V
I_{LK}	Input Leakage Current	V_{IN} = 0V to V_{DD}, see Note 2	-10		10	µA
C_{IN}	Input Capacitance			3.5		pF
I_{OL}	Output Sink Current	V_{OL} = 0.5V		10		mA
t_{SP}	Pulse Width of Spikes which must be suppressed by the Input filter		0		50	ns
f_{SCL}	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time between a STOP and START Condition		1.3			µs
$t_{HD,STA}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.		0.6			µs
t_{LOW} t_{HIGH}	Low Period of the SCL Clock High Period of the SCL Clock		1.3 0.6			µs µs
$t_{SU,STA}$	Set-up Time for a repeated START Condition		0.6			µs
$t_{SU,STO}$	Set-up Time for STOP Condition		0.6			µs
$t_{HD,DAT}$	Data Hold Time	See Note 3	0		0.9	µs
$t_{SU,DAT}$	Data Set-up Time	See Note 4	100			ns
t_R, t_F	Rise and Fall Time of both SDA and SCL signals	See Note 5	20 + 0.1 C_B		300	ns
C_B	Capacitive Load for each Bus Line				400	pF

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Notes : 1. An impedance higher than 2kΩ is required when SDA and SCL are tied to a 5V ± 10% voltage line.

2. Leakage current exceeds ± 10µA when SDA and SCL are tied to a 5V ± 10% line.

3. A device must internally provide a hold time of at least 300ns for the SDA signal (refered to the $V_{IH\ Min.}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
The maximum tHD,DAT has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

4. A fast-mode I^2C bus device can be used in a standard-mode I^2C bus system, but the requirement $t_{SU,DAT} \geq 250ns$ must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ Max.} + t_{SU,DAT} = 1000 + 250 = 1250ns$ (according to the standard-mode I^2C bus specification) before the SCL line is released.

5. C_B = total capacitance of one bus line in pF.

Figure 4

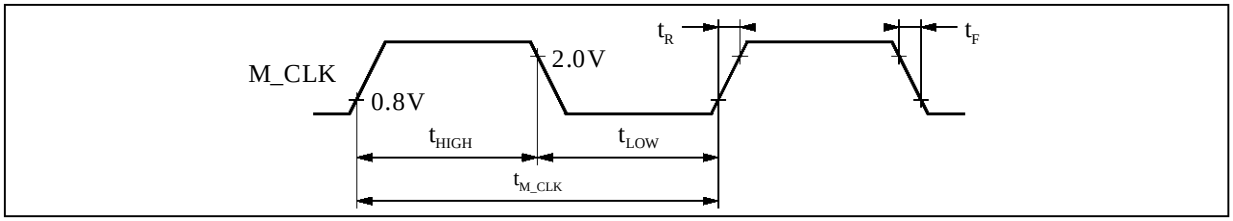


Figure 5

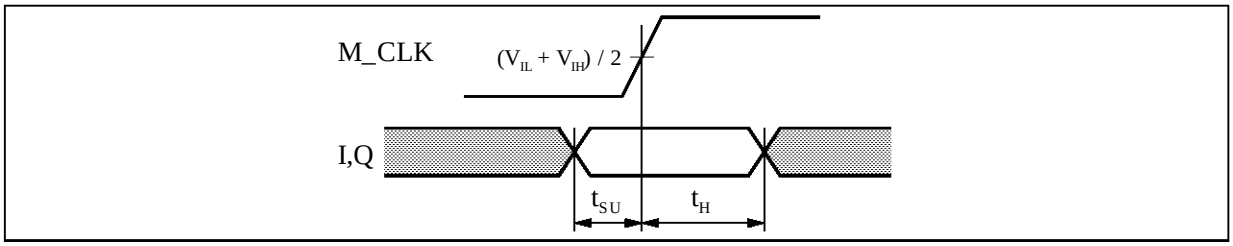


Figure 6

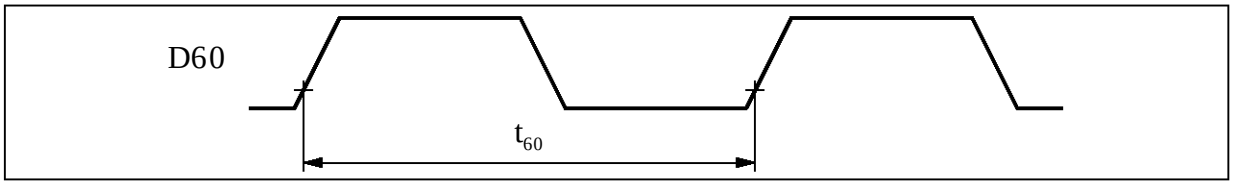


Figure 7

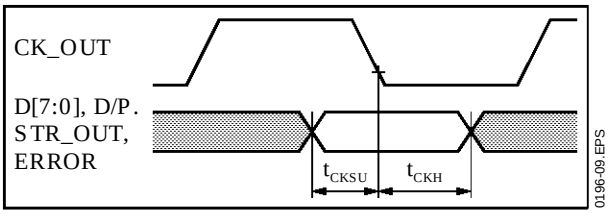


Figure 8

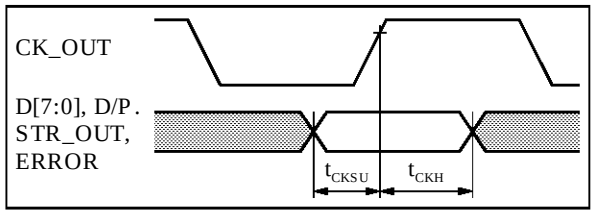
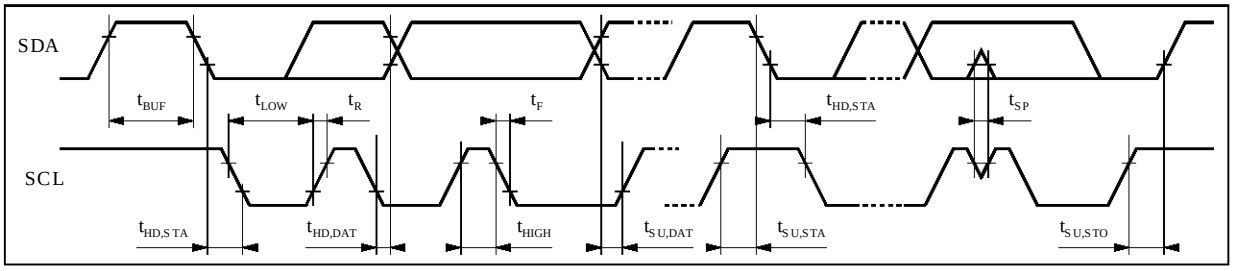
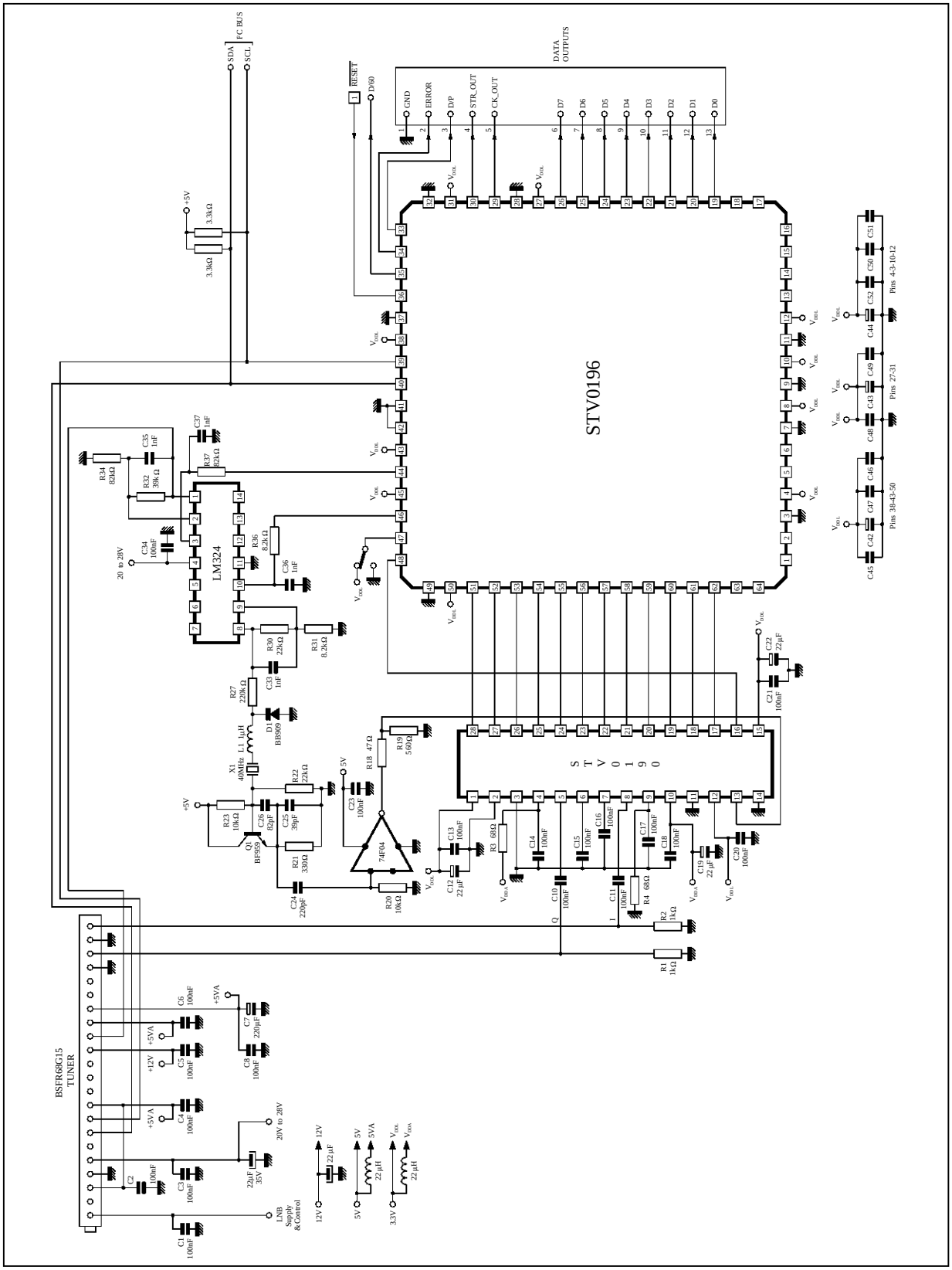


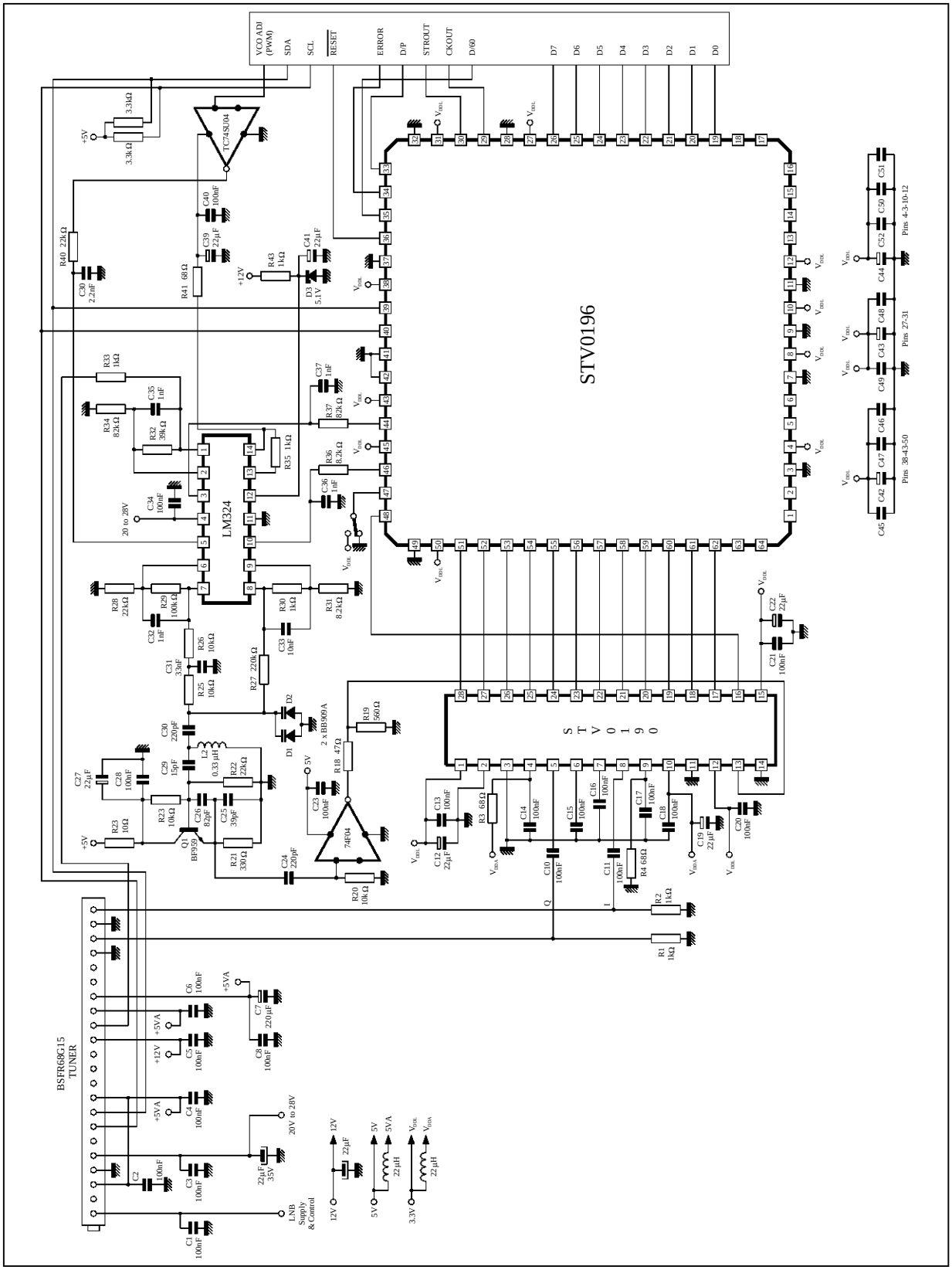
Figure 9



APPLICATION DIAGRAM : STV0196/STV0190 Fixed 20 MBauds Application

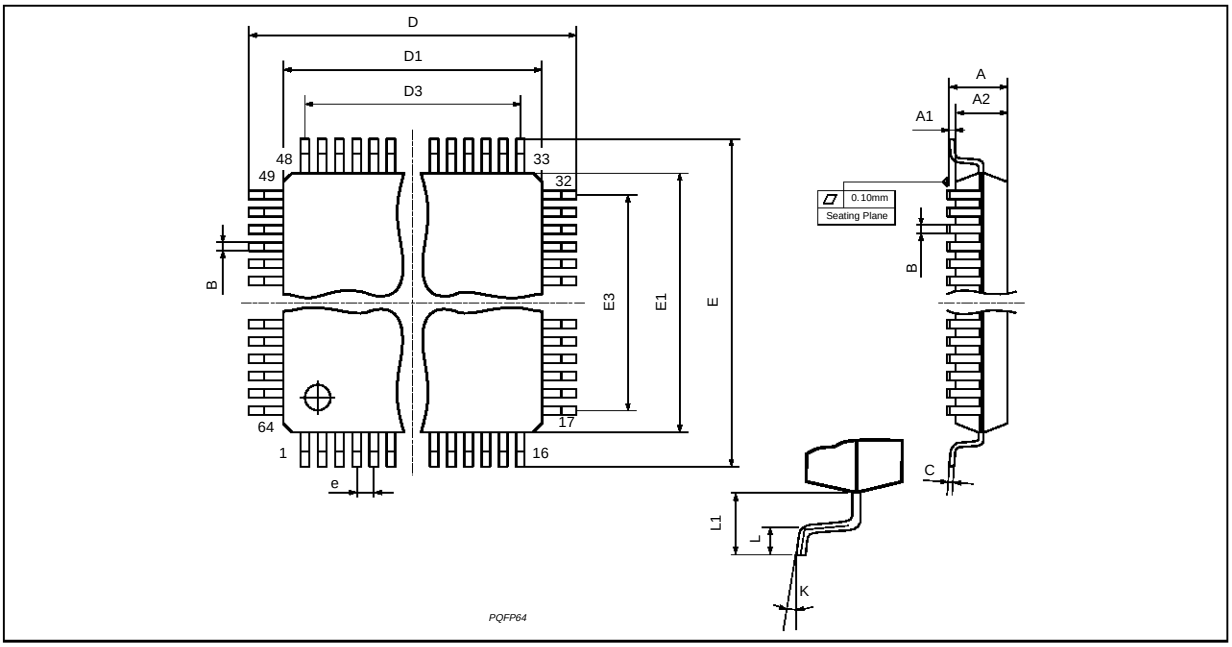


APPLICATION DIAGRAM : STV0196/STV0190 Multirate Application



PACKAGE MECHANICAL DATA

64 PINS - PLASTIC QUAD FLAT PACK



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.30		0.45	0.0118		0.0177
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D3		12.00			0.472	
e		0.80			0.0315	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
K	0^o (Min.), 7^o (Max.)					
L	0.65	0.80	0.95	0.026	0.0315	0.0374
L1		1.60			0.063	

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